High-Resolution Multi-Channel FPGA-TDC Architectures

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Motivation

FPGA-TDC:

- Fast development process
- Flexible (Clock frequency, resolution/channel Nr. trade-off)
- Adaptable (Special needs, e.g: extra large FIFOs for bursts)

Previous work in this field, e.g.:

- 1997: Kalisz, Altera Quick Logic, 200 ps resolution
- 2008: J.Wu, Altera-Cyclone-II, 10 ps RMS
- 2009: Favi, Virtex-5, ~ 17 ps resolution
- 2010: Bayer, Virtex-4, 9 ps RMS

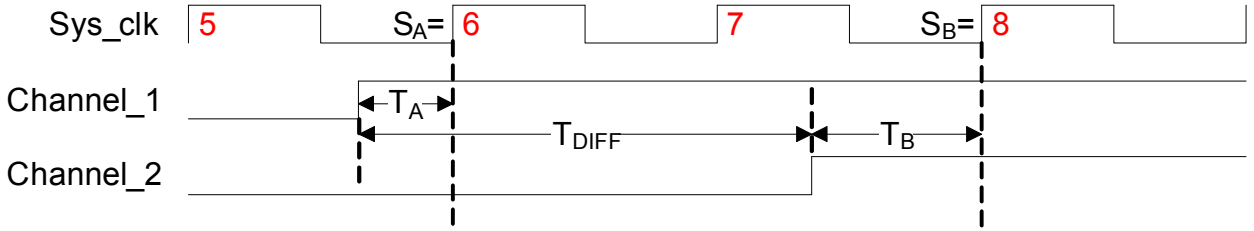
Time Measurement

Sampling with system clock:

- Only one FF per channel.
- Uncertainty: sys_clk_period

The Nutt method:

- 1 Stage: Counter
- 2 Stage: Interpolator

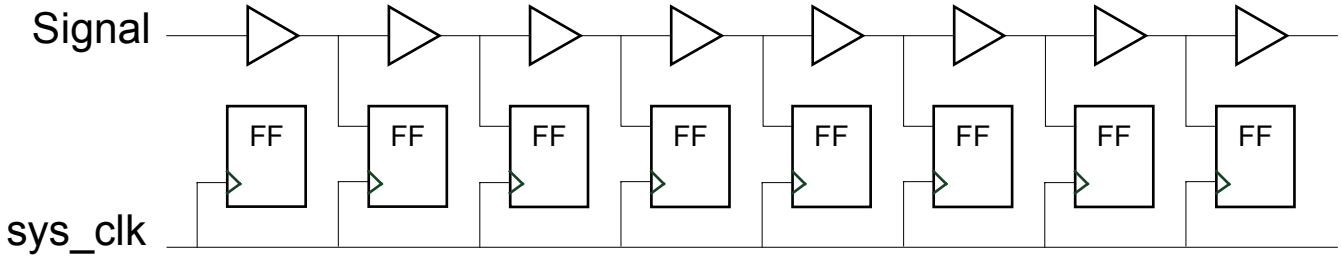


$$T_{DIFF} = T_A + (T_{SYS} - T_B) + (T_B - T_A - 1) \cdot T_{SYS}$$

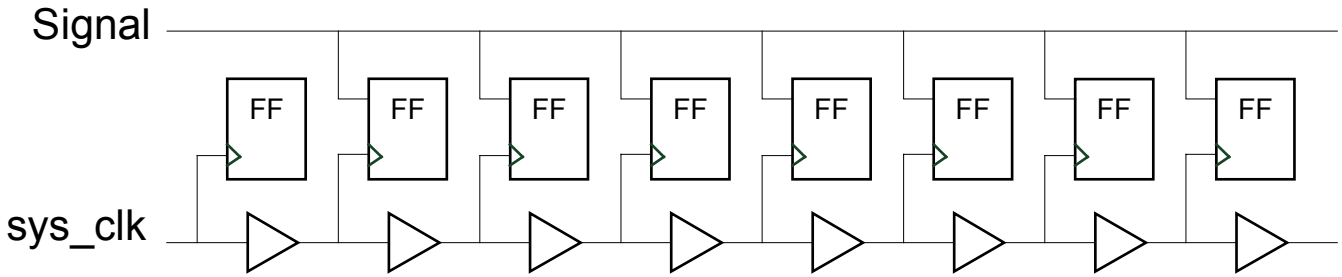
$$T_{DIFF} = T_A - T_B + |S_A - S_B| \cdot T_{SYS}$$

Interpolation Methods – Tapped Delay Lines

1.



2.



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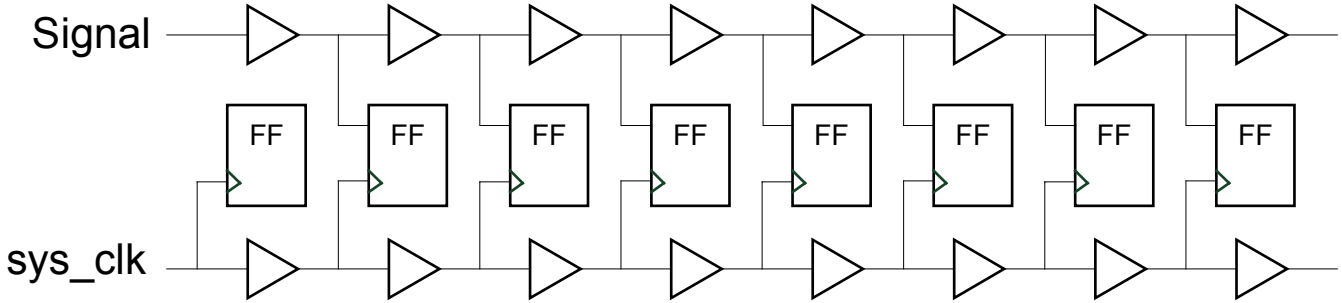
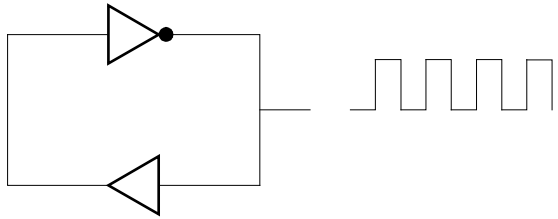
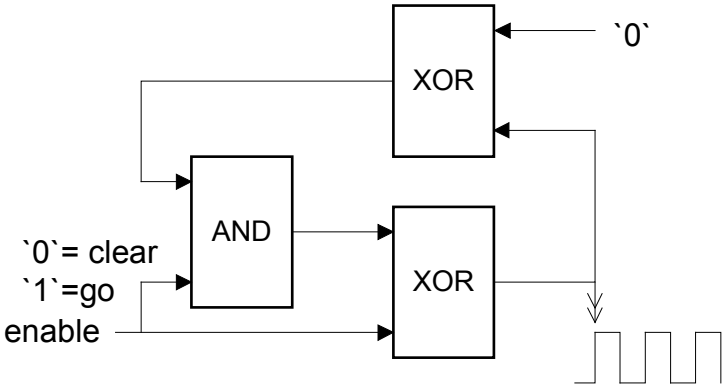


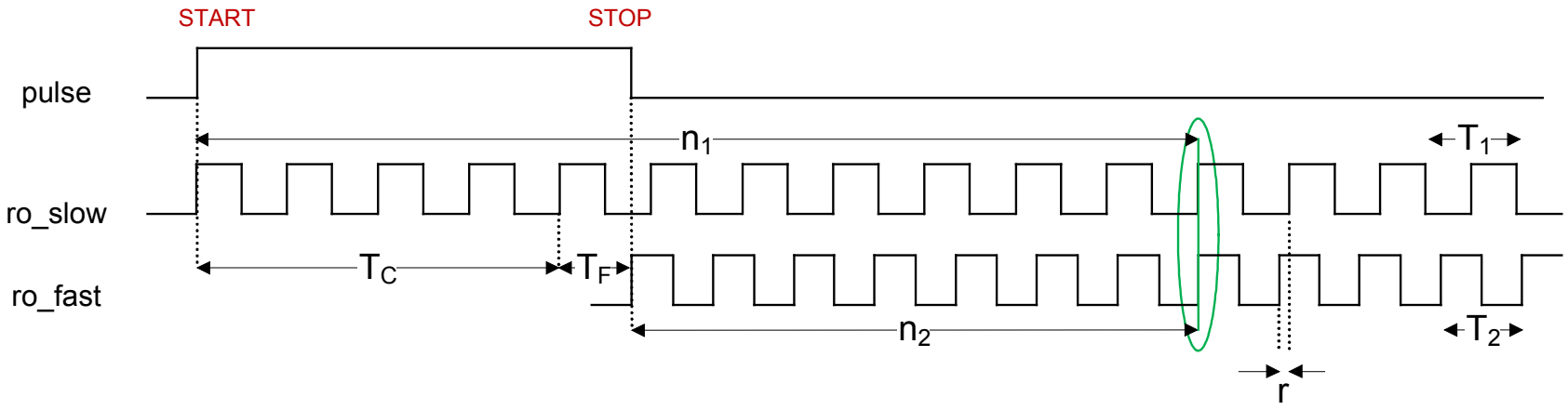
Interpolation Methods – Ring Oscillators

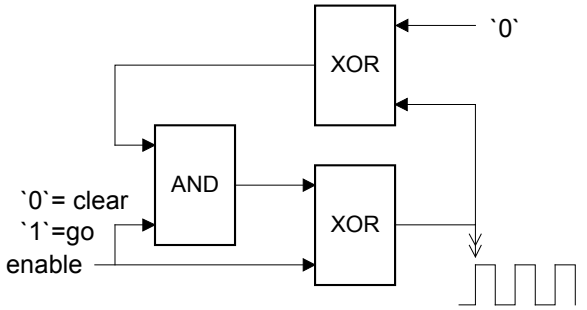




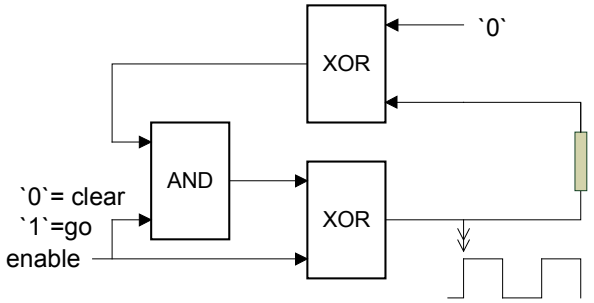
in_2	in_1	XOR	
0	0	0	Follower
0	1	1	
1	0	1	Inverter
1	1	0	

Interpolation Methods – Vernier Method





ro_fast



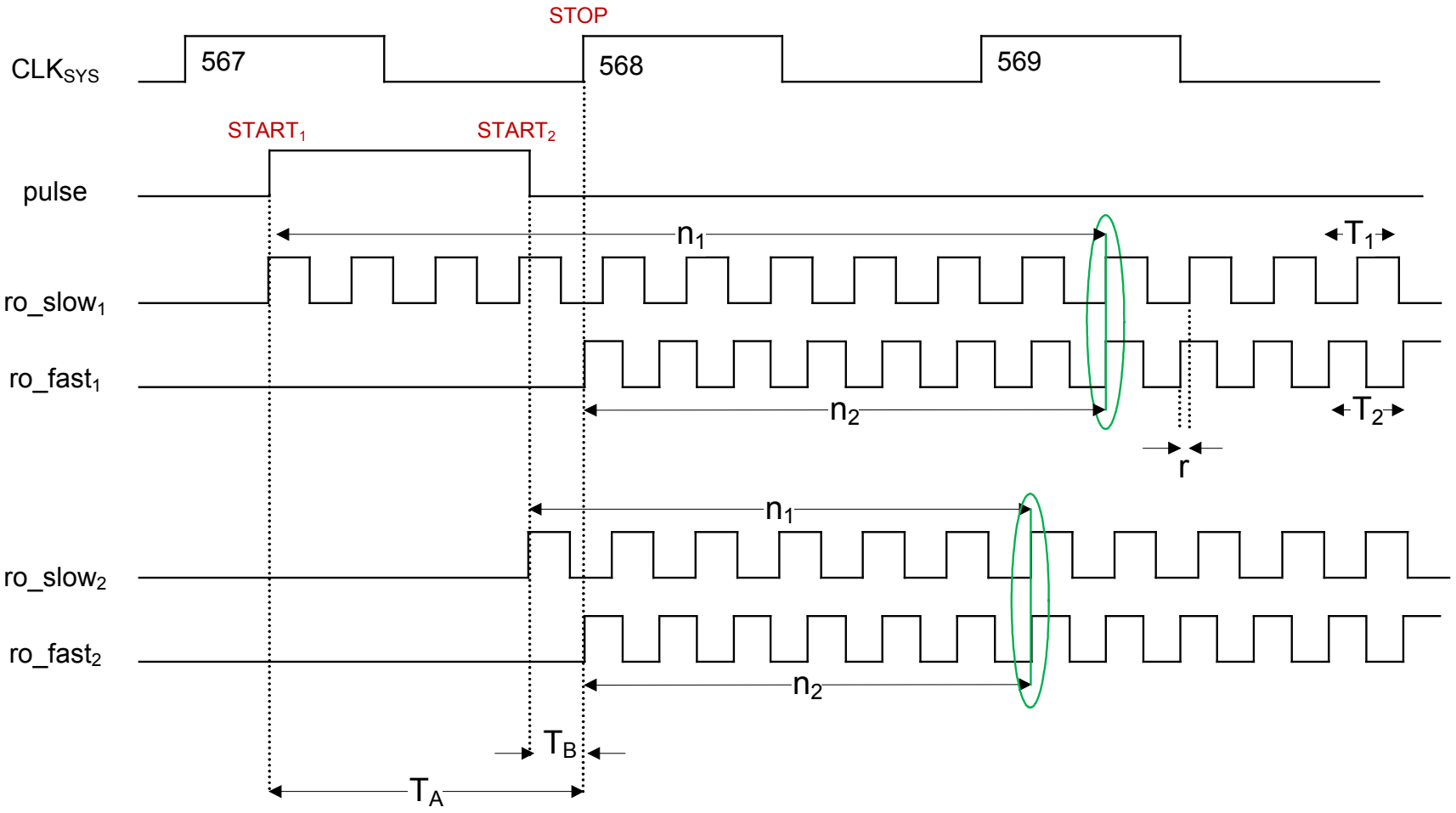
ro_slow

$$T_P = T_C + T_F$$

$$T_C = (n_1 - n_2) \cdot T_1$$

$$T_F = (n_2 - 1) \cdot r$$

Vernier + Nutt Method



Here: $\text{timestamp}_A = \text{timestamp}_B \rightarrow T_P = T_A - T_B$

Interpolation Methods in FPGAs

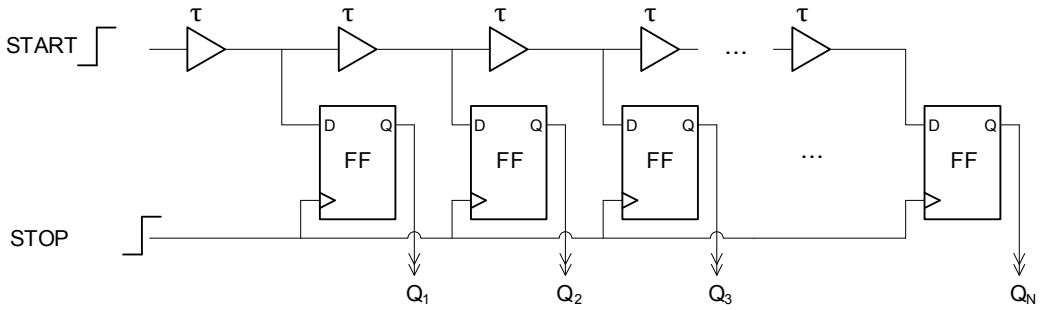
Ring Oscillator based:

- Difficult to implement due to routing delay unpredictability.
- Non stochastic jitter of the RO-Signal → Large accumulated jitter.
- Implementation of multi channel TDCs based on the Vernier-RO method is complex and time consuming.

Tapped Delay Lines based:

- A large effort was done by the vendors to distribute the system clock signal on the FPGA die with the minimal skew.
- On modern FPGAs many dedicated carry lines are available which are designed to be as fast as possible to implement fast carry adders.

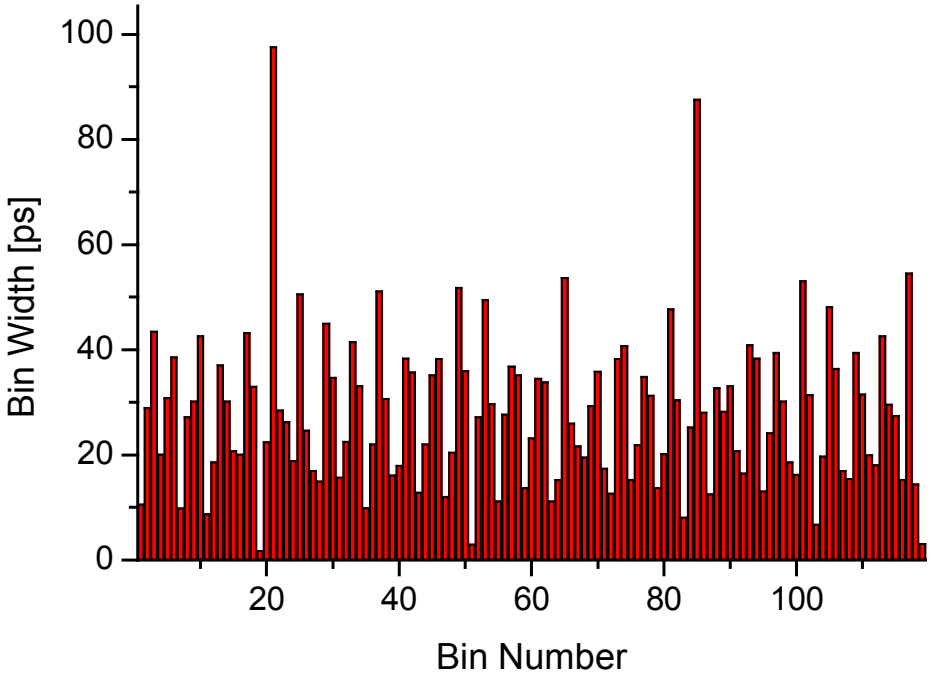
→ TDL method 1 can be implemented with the minimal effort on time.

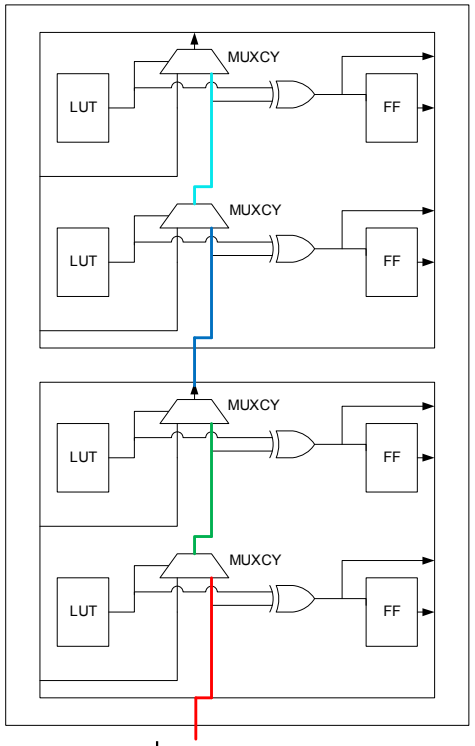


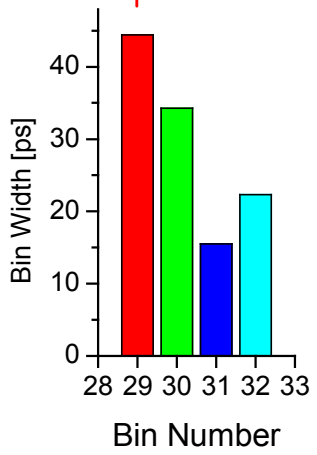
Tapped Delay Lines in FPGA

FPGA:

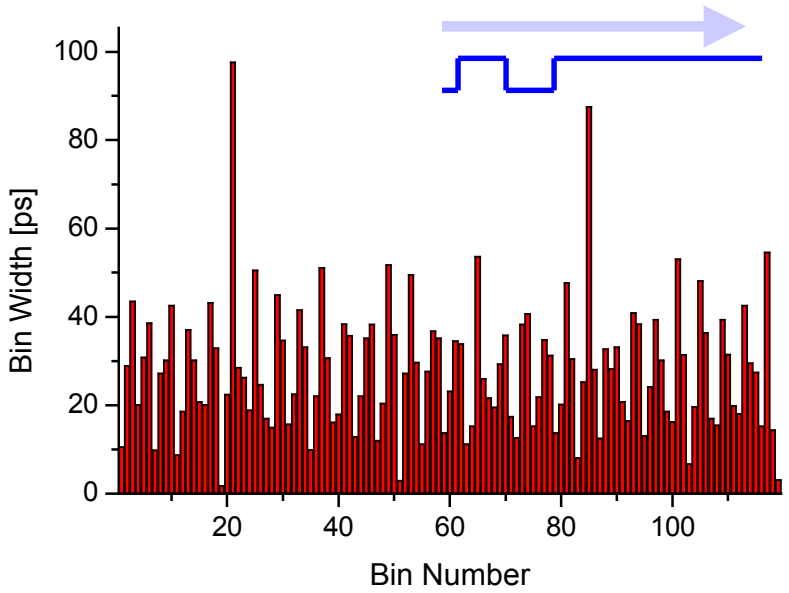
- The "Carry-Chain" serves as a delay chain
- Carry-Chain multiplexers are the delay elements
- Delay (max.) = 45 ps (Virtex-4: CIN→COUT = 90 ps, speed grade 10)
- Real delays vary → cell-by-cell calibration necessary







Wave Union Method



Wave Union Method:

- Two or more transitions propagate.
- If one transition is in an ultra wide bin, then the other is in a normal bin.

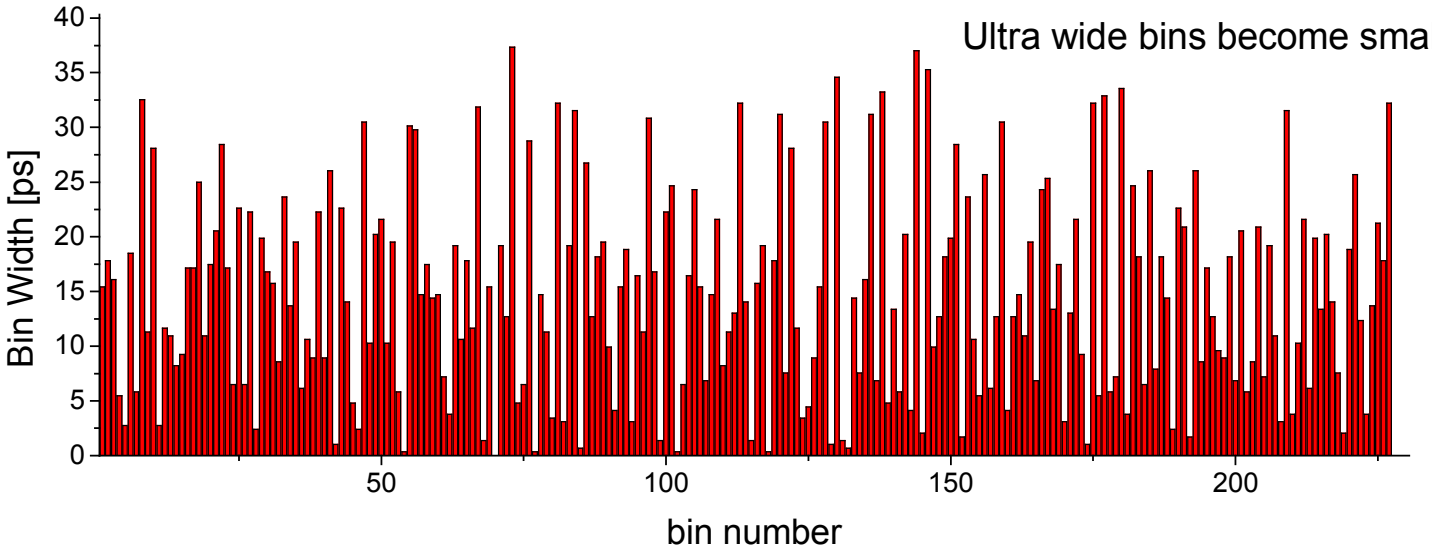
Procedure:

- Store a pattern of edges
- Trigger them simultaneously

  →Control the runtime of signals (difficult but feasible)

Consequence:

Ultra wide bins become smaller.



Calibration

- Can be done in software or hardware (inside FPGA)
- Hardware → additional resources needed
- Software:
  - Saves resources for additional channels
  - Simple algorithm:

1. Code Density Test (uncorrelated cal. signal or book real hits)
2. Calculate the width of each bin in ps

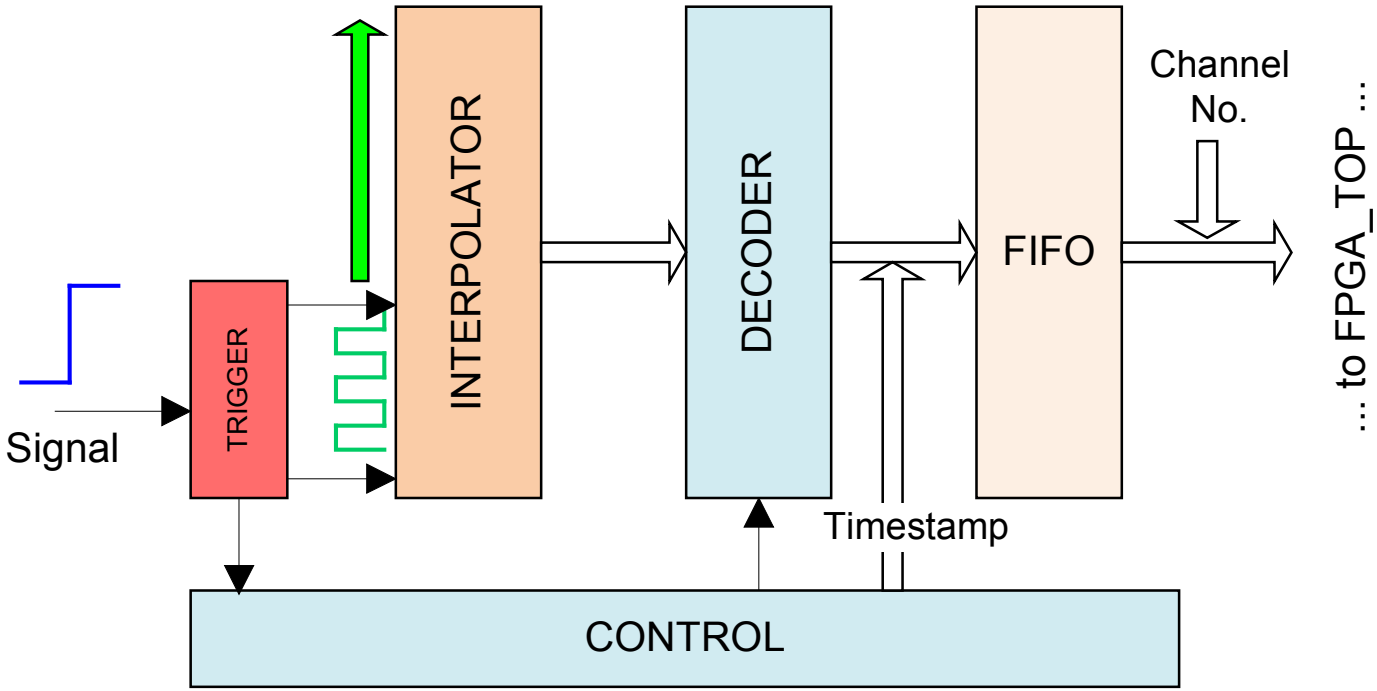
$$w_i = \frac{n_i}{N} \cdot 5000\,ps \qquad N = \textit{total number}$$

3. Construct the Conversion-LUT:

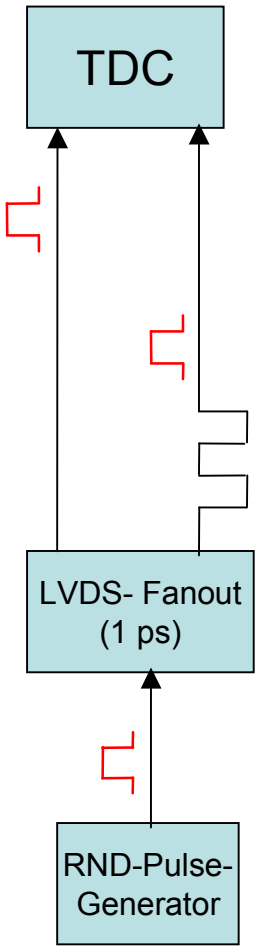
$$b_i = \left(\sum_{k=1}^{i-1} w_k \right) + \frac{w_i}{2}$$

Design (one TDC-channel, simplified)

- TDL method extended with “Wave Union” method [Wu]
- Pipelined design
- Dead time > 15 ns (depends on needed resolution).
- Puffer for 512 hits per channel.
- Real rate depends on readout interface.



Measurements

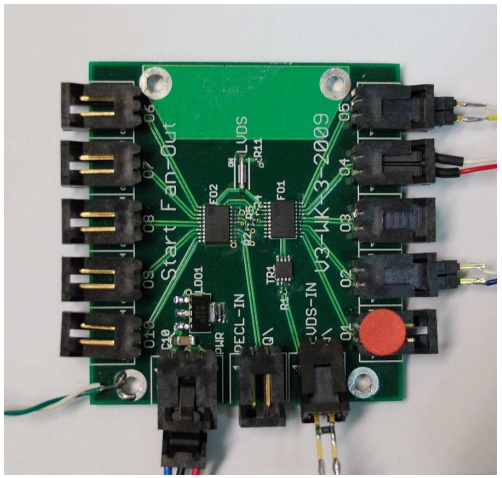


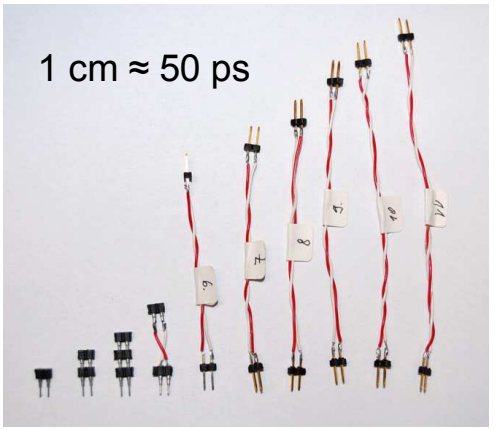
Measured:

1. Root Mean Square $RMS = \sqrt{\frac{\sum_{i=1}^{N}(x_i - \bar{x})^2}{N}}$
2. Temperature dependence
3. Dependence on the supply voltage variations
4. Crosstalk

Measurement setup:

- Delay between 2 rising edges on different channels
- ~ 250k measurements / setup.
- Delays < 1 ns were adjusted via different cable lengths
- Delays > 1 ns were adjusted with the Tektronix Data Timing Generator (precision = 1 ps)
- Measurement value: prop. status + timestamp
- Calibration and analysis offline



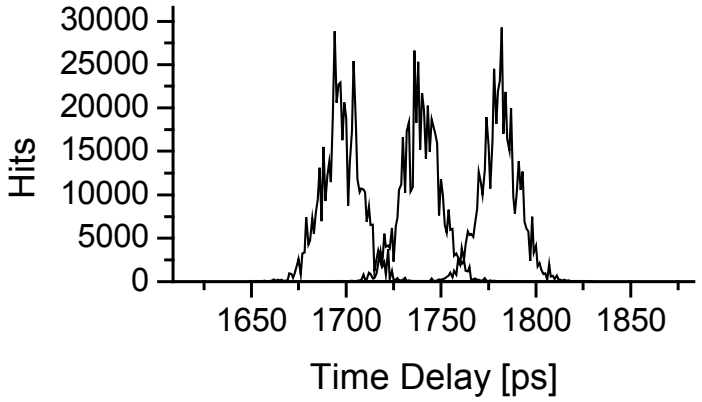


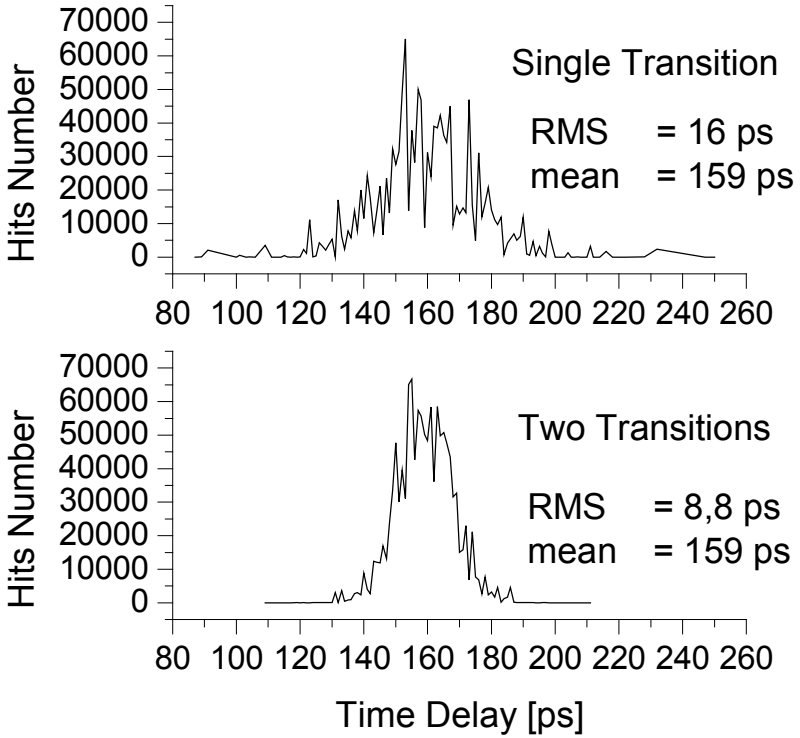
RMS

- **3 measurement series:** the async. edges arrive...
  1. ... within one period of the system clock.
  2. ... with an offset of multiple sys_clk cycles.
  3. ... with offset > 1 µs.
- **Test reading:**

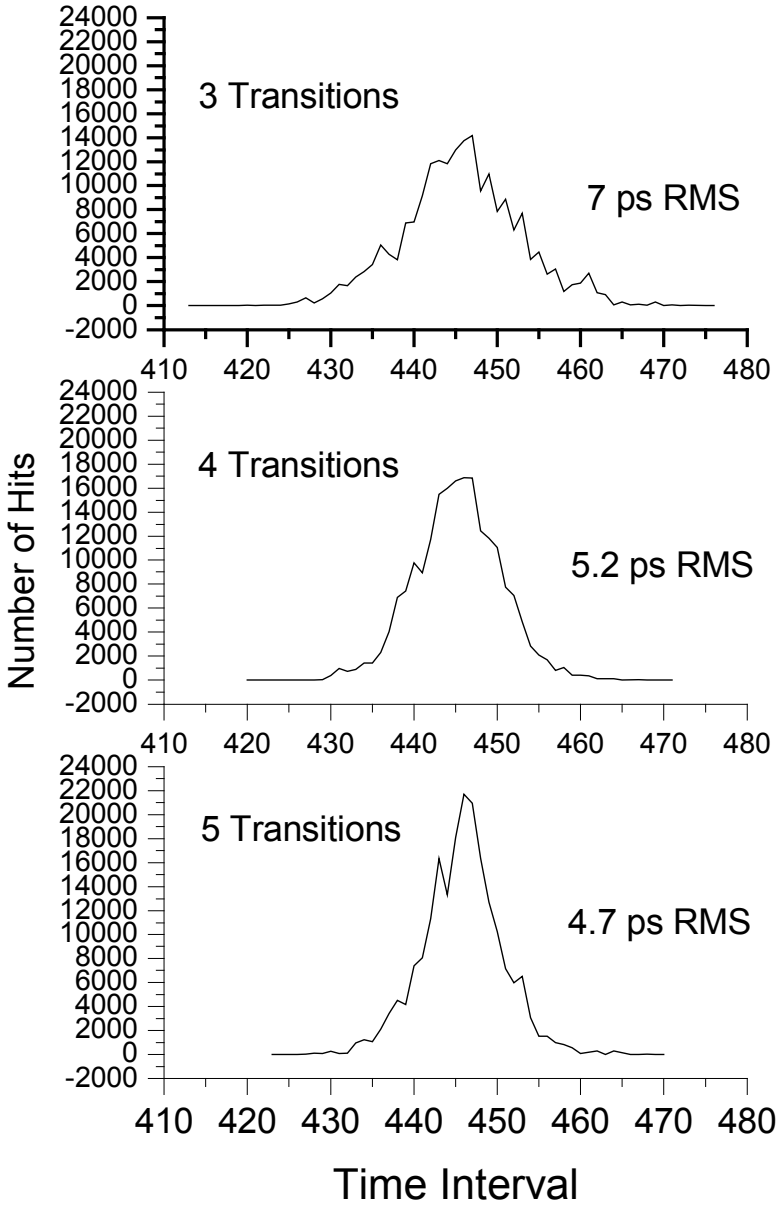
wire length channel A	mean [ps]	RMS [ps]
~6 cm	1697	9
~7 cm	1740	9
~8 cm	1781	9

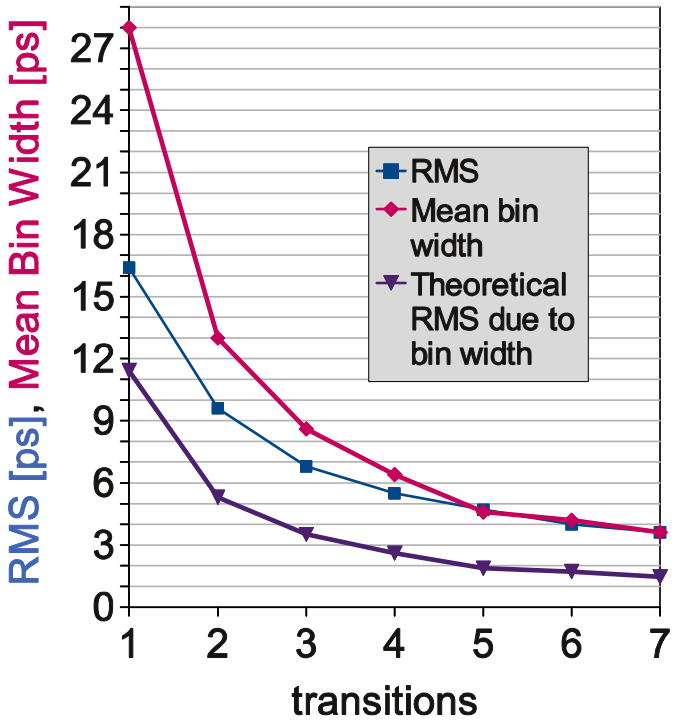
DTG time diff. [ns]	mean [ps]	RMS [ps]
42	45798	9
44	47798	9
46	49798	9
1004	1005795	11
1006	1007797	11
1008	1009798	11





RMS - improved

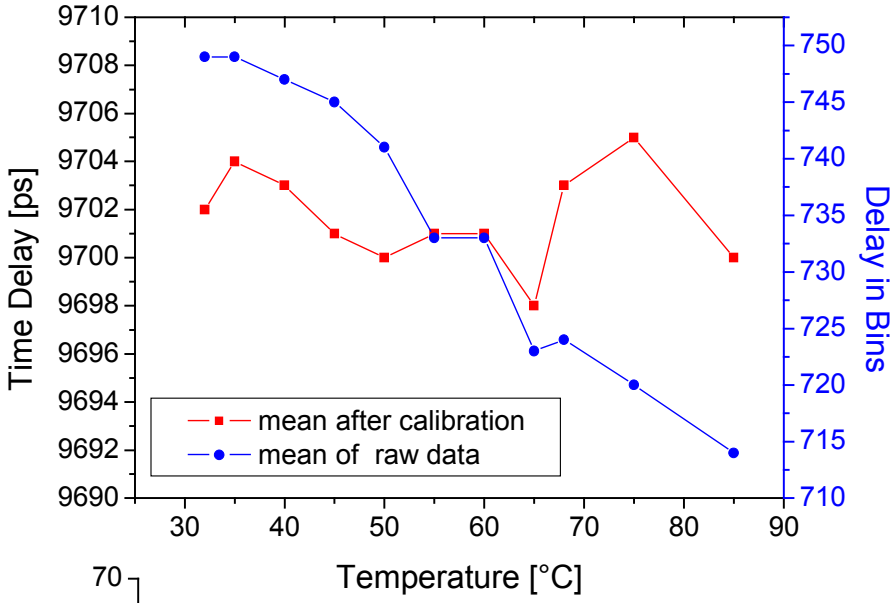


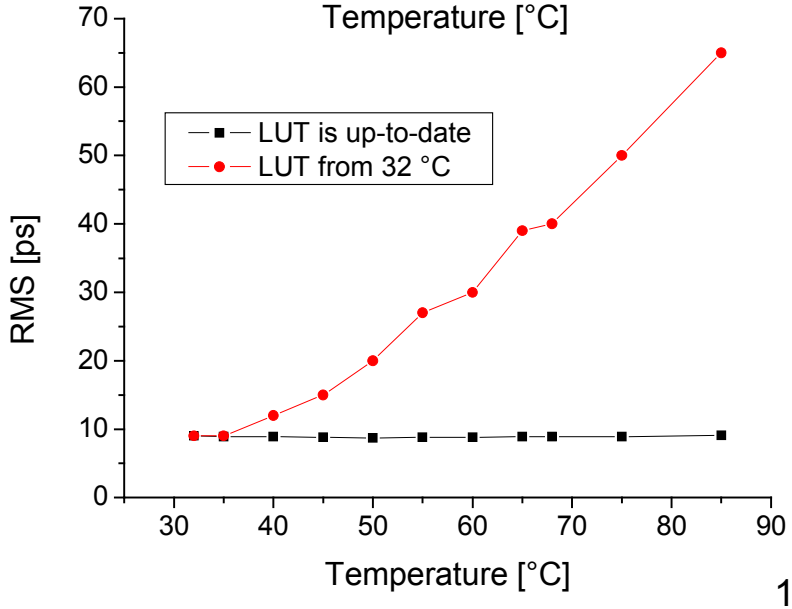


Temperature Variation

- **Temperature region:** 30 °C – 85 °C in 5°C steps.
- **Observations:**
  1. Deformation of the calibration LUTs.
  2. Measured distance in delay elements changes, but...
  3. ...no change of the calibrated value of the RMS, if calibration LUT is up-to-date. (acceptable region: ± 5°C)
- **Conclusion:**

  No significant effect!

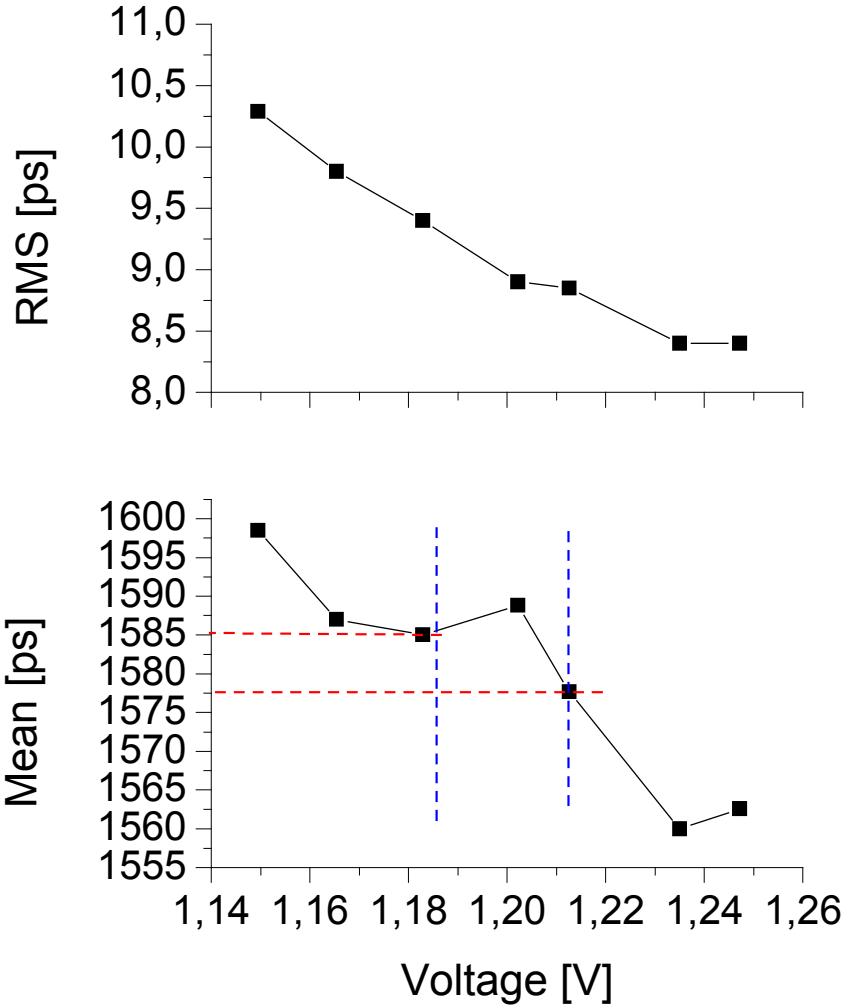




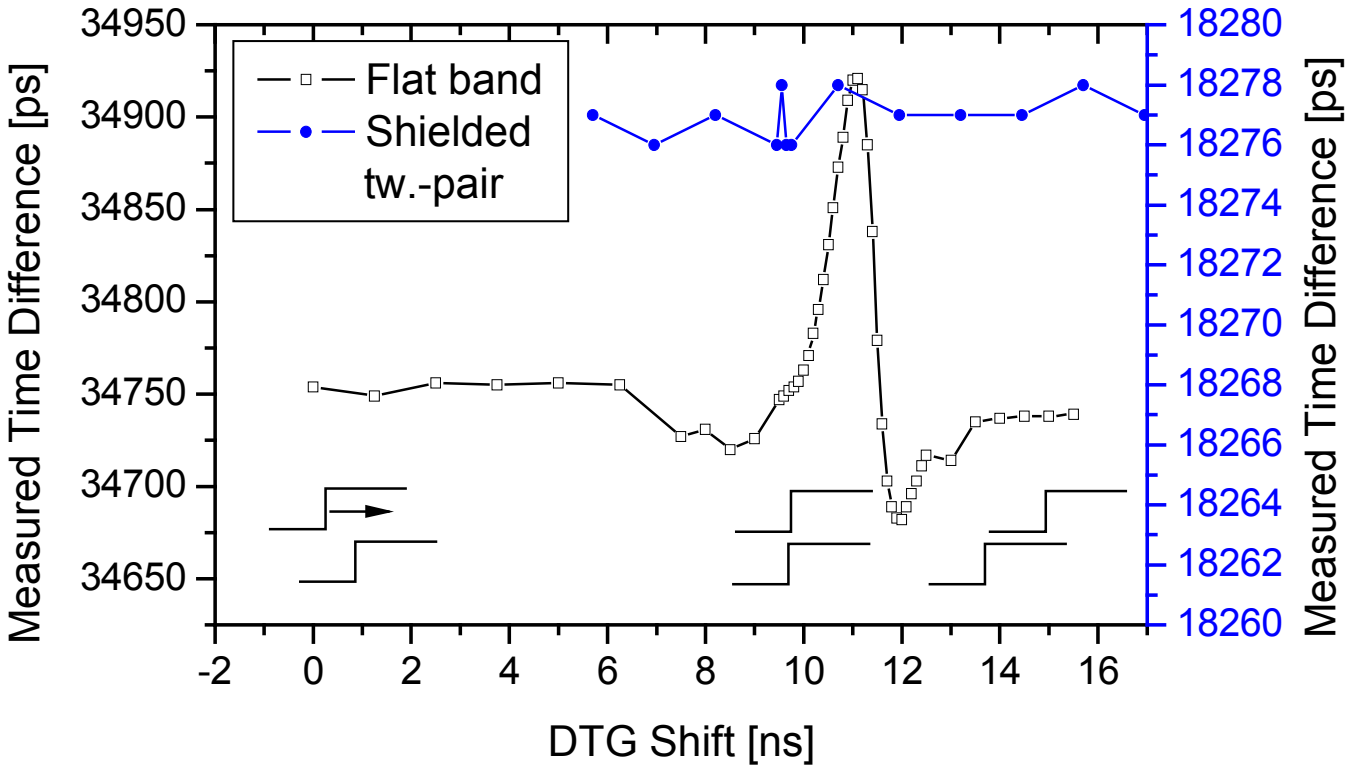
Core Voltage Variation

- **Region :** 1.15 V – 1.25 V
- **Observations:**
  1. Deformation of the calibration LUTs
  2. 2 ps increase of the RMS value
  3. 40 ps shift of the mean in the whole region
- **Conclusion:**
  - The voltage has to be stabilized
  - Worst case ± 12 mV

    → ca. 7 ps
  - (Normal case: ± 2 mV)



Crosstalk



- No crosstalk under normal conditions
- Prove of sensitivity with enforced crosstalk (flat band cable)

→ NO CROSS TALK INSIDE FPGA

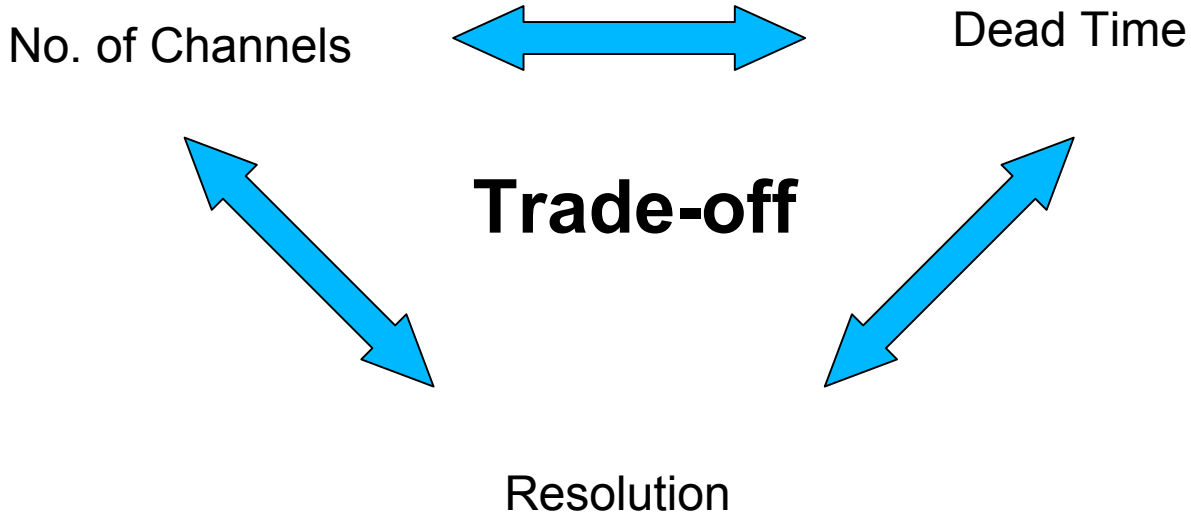
Usage of Resources

- 50 channels (10 ps RMS) on XC4VLX40 with 40k logic cells.
- 10 channels (3.6 ps RMS) on the same FPGA @ 50% resource usage.

→ Geometry of the FPGA die is also a factor.

- Up to 200k logic cells on one FPGA in this FPGA family.
- Resource usage decreases in newer FPGA families due to optimized FPGA architecture.

Design Options



Dead time:	10 ns @ 16 ps RMS ←→ 50 ns @ 3.6 ps RMS
	or >1 GHz with a reduced number of channels.
No. of ch.:	depends on FPGA (~ up to 128 of 10 ps RMS ch.)
Resolution:	3.6 ps RMS resolution achievable

High flexibility!

Comparison with other TDCs

FPGA-TDC (GSI):

- ~48 channels with 9 ps RMS or 32 channels with 5 ps RMS for a time interval measurement, dead time: 3 cycles @ 200 MHz = 15 ns.

FPGA-TDC (J.Wu):

- 18 channels with 25 ps RMS, dead time: 2 cycles @ 400 MHz
- 8 channels with 10 ps RMS, dead time: 18 cycles @ 400 MHz

HP-TDC (CERN):

- 32 channels with 30 ps resolution
- 8 channels with 17 ps resolution

TDC-GPX (ACAM):

- 8 channels with 27 ps resolution, 200 MHz max. Hit rate (40 MHz continuous)
- 2 channels with 10 ps resolution, dead time 18 cycles, 500 kHz continuous hit rate

Thanks for your attention!